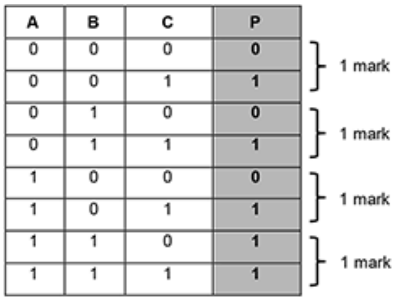
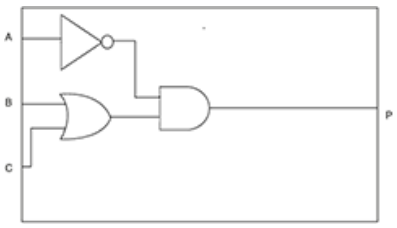
# Mark scheme

| Question | | | Answer/Indicative content | Marks | Guidance |
|---|---|---|---|---|---|
| 1 | a | | 1 mark per group of 2 rows<br>  <br> | 4<br>(AO2) | Accept True / False etc. |
| | b | | 1 mark each<br>• NOT A<br>• B OR C<br>• AND gate with **two inputs**<br>  <br> | 3<br>(AO3) | **Max 2** if not logically correct or any additional / missing gates.<br><br>Shapes of gates must be correct with correct number of inputs. Ignore annotation of gate names.<br><br>NOT gate must include circle. Other gates must not include circle.<br><br>**Examiner's Comments**<br><br>Drawing logic circuits is now a commonly asked question and candidates are generally competent at doing this. Where issues did arise, they tended to be missing the circle from the NOT gate (and therefore turning it into a buffer, not a logic gate) or including the incorrect number of inputs into a gate.<br><br>**Key point – logic gates**<br><br>Candidates are expected to be able to draw the correct shapes for each gate. A number of candidates labelled their gates up, but this is not necessary; examiners are instructed to mark the shape of each gate and ignore any labelling.<br><br>Candidates are **not** allowed to take stencils or other tools that allow them to more easily draw these gates into an examination unless as part of a |

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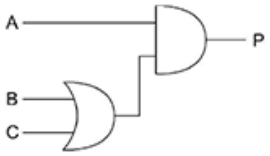
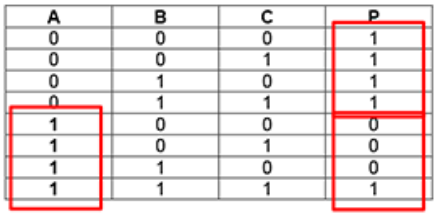
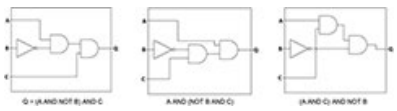
| | | | | | specific access arrangement agreed by OCR. |
| | | | **Total** | **7** | |
| 2 | a | | • B OR C<br>• AND gate with A as one input…<br>• …and output of BP1 as other input | 3<br>(AO2 1b) |  <br><br>Mark shape of gates, ignore candidate annotation. |
| | b | | One mark per highlighted section<br>  | 3<br>(AO1 1a, AO2 1a) | |
| | | | **Total** | **6** | |
| 3 | a | | 1 mark each, max 2 if not fully correct circuit.<br>• NOT B<br>• AND gate with A / C as one **direct** input…<br>• …Second AND gate with other (unused) A / C as **direct** input **and** output of previous stage as other input<br><br>Fully correct circuit is any of :<br>• Q = (A AND NOT B) AND C<br>• Q = A AND (NOT B AND C)<br>• Q = (A AND C) AND NOT B<br><br>See examples below :<br>  | 3<br>(AO3 2a) | Shapes of logic gates must be correct. NOT gate must include circle for inversion. No other gates should include circle.<br><br>AND gates must have two different inputs, NOT gate must have one input. All gates must have one output.<br><br>Correct system will always have **NOT B** and two other AND gates correctly joined.<br><br>Accept alternative systems that produce the correct output.<br><br>Accept (BOD) three input AND gate for BP2 and BP3 if used correctly.<br><br>OK if inputs/outputs not joined up to A/B/C/Q as long as intention clear.<br><br>If lines cross on diagram, give BOD.<br><br>If (A AND C) AND NOT B drawn, allow NOT B as first input for BP3.<br><br>**<u>Examiner's Comments</u>**<br><br>This logic question is based around a |

| A | B | C | P |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

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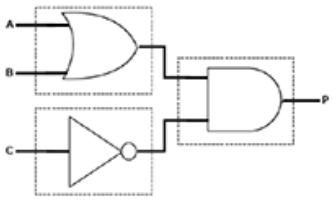
| | | | | | typical outdoor light system. The majority of candidates were able to show understanding that both the switch (input C) and the motion sensor (input A) need to be triggered for the light (output Q) to be on. However, some candidates missed the description that this only occurs at nighttime. Input B is the light sensor and so a NOT gate is required on this input to fulfil this requirement.<br><br>Given that AND gates generally have two inputs and this system uses three inputs, two AND gates were required. The mark scheme credits any and all arrangements of these to reach the correct output.<br><br>Examiners were also instructed to credit use of a 3 input AND gate. |
| | b | | 1 mark each<br><br>• Logic gate 1: **OR**<br>• Logic gate 2: **AND** | 2<br>(AO2 1a) | Allow **A OR B / B OR A** for logic gate 1<br>Allow **A AND B / B AND A** for logic gate 2<br><br>If logic statement provided with multiple gates (e.g. A OR B AND C) this is incorrect.<br><br>Allow use of symbols (e.g. ∨, + for OR, ∧, . for AND)<br><br>Allow correct drawing of logic gates. |
| | | | **Total** | **5** | |
| 4 | | i | • A **OR** B<br>• **NOT** C<br>• **AND** gate<br><br>  <br> | 3<br>(AO2 1b) | 1 mark per gate. Correct symbols must be used.<br><br>**NOT** gate must have circle for inversion**, OR** and **AND** must not have a circle<br><br>Mark the **shape** of each gate, not the name written if given. Ignore any writing / notes.<br><br>Lines do not have to be drawn or joined up, but if they are, gates must have the **correct number of inputs/outputs.** Penalise once then FT**.** |

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| | | | | | **Examiner's Comments**<br><br>This question was answered extremely well. Candidates were familiar with the logic symbols required for each gate.<br><br>A few candidates missed the circle from the NOT gate symbol (which turned this into a buffer instead) or added a circle to the AND and OR gates. This turned them into NAND and NOR gates. These logic gates are not on the GCSE specification, but are covered at A Level. Teachers may find it beneficial to briefly discuss these in order to anticipate mistakes like these.<br><br>A small number of candidates drew indistinct logic gate symbols and named them instead, such as a rectangle with AND written in; this was not credited with a mark. |
| | | ii | • To show **all possible inputs** (to the logic circuit)…<br>• **…**and the **associated/dependent** output (for each input) | 2<br>(AO1 1b) | For 2nd BP, must be clear that the output is linked to the input values given.<br><br>"All possible combinations of inputs and outputs" gains the first mark (all possible inputs) but not the second.<br><br>**"**The output **for** each possible input" gains both marks<br><br>**Examiner's Comments**<br><br>It is clear that candidates have experienced and used truth tables with logic circuits. However, the majority were not able to describe the truth table's purpose with precision.<br><br>A truth table defines the expected outputs for a logic circuit depending on the inputs given. Furthermore, the truth table covers all possible permutations of inputs. |

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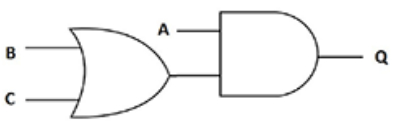
| | | | | | A logic circuit with three inputs (A,B and C) will have **8** possible rows in a truth table to cover the 8 possible ways that True and False values for three inputs can be arranged.<br><br>**Misconception**<br><br>The number of rows in a truth table depends on the number of inputs. The number of rows can be given by $2^x$, where x is the number of inputs. Therefore, a truth table with 3 inputs would have $2^3$ rows, or 2 × 2 × 2 = 8 rows.<br><br>Exemplar 1<br><br>To show what output happens for every variation of inputs, and check they are all what was intended<br><br>Here the candidate has achieved both marks available; it is clear that every variation of input is included in the truth table and the output is very clearly linked to these inputs. |
| | | iii | • 8 / eight | 1<br>(AO2 1a) | Accept other answers that equate to 8 (e.g. $2^3$) |
| | | | **Total** | **6** | |
| 5 | | | <table><tr><th>A</th><th>B</th><th>P</th></tr><tr><td></td><td></td><td></td></tr><tr><td></td><td></td><td>1</td></tr><tr><td></td><td></td><td>1</td></tr><tr><td></td><td></td><td></td></tr></table> | 2<br>(AO1 1b) | 1 mark for each correct answer in table<br><br>'True' or 'T' are also credit worthy. |
| | | | **Total** | **2** | |
| 6 | | | • OR gate with two inputs / AND gate with two inputs<br>• Diagram as shown in guidance with no additional gates | 2 |  |
| | | | **Total** | **2** | |